UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,548	03/08/2002	Junichi Kimura	2002_0188A	8800

513 7590 07/14/2004

WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,548	KIMURA, JUNICHI	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,19,21-26 and 28-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,19,21-26 and 28-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 46 and 48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Newly added claims, 46 and 48, which recite the thermal expansion coefficient of the resin and the board render new matter.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 18-19, 21-23, 28-39, and 41-43, 45, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino (US 6,545,353, previously cited) and in view of Glenn et al. (US 6,291,884, newly cited, hereinafter, Glenn.)

In regard to claims 18, 31-32, 36, 43, 45, and 47, in fig.1, Mashino disclose a layer 102 having a first side and a second side opposite said first side, the ceramic layer inherently having a dielectric constant;

an impedance element on said ceramic layer, for example, 104;

a first resin layer 105 over said first side of said ceramic layer, the first resin layer inherently having a dielectric constant lower than said dielectric constant of said ceramic laver;

a second resin layer, also, 105 over said second side of said ceramic layer;

a third resin layer over said first resin layer, also, 105; and

a strip line 106, for example, on said first resin laver.

Mashino, however, does not disclose that layer 102 is made of ceramic. It should be noted that ceramic is widely used to make PCB to carry semiconductor chip because it has closer thermal coefficient to silicon chip, therefore, preventing wrap between devices. For instance, Glenn discloses an analogous device having chip 104 attached to a ceramic substrate 126. The ceramic and other materials including therein are used to have a similar TCE to the chip in order to prevent cracking, reducing cost and thermal resistance between the chip and the substrate. See col. 5, lines 1-29.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to substitute the material of the substrate as taught by Glenn in order to prevent cracking, reducing cost and thermal resistance between the chip and the substrate.

In regard to claims 19, 33, Mashino further discloses an electronic component mounted on said first resin layer, for example, part of the element 106.

In regard to claim 21, Mashino further discloses a strip line on said third resin layer, also, 106.

In regard to claims 22, 38, wherein an electronic component, also, part of 106 mounted on said third resin layer.

In regard to claims 23 and 39, Mashino discloses a fourth resin layer, also, 105.

In regard to claims 28, 30, elements 104 and 112b of Mashino function as resistors; see fig. 2a.

In regard to claim 35, Mashino discloses a strip line on said second resin layer, also, 106.

In regard to claim 36, Mashino discloses a third resin layer over said first resin layer, also, 105.

In regard to claim 37, Mashino discloses a strip line on the third resin layer, also, 106.

In regard to claims 29 and 41 the processing limitations recited (laser-trimmed), this would not carry patentable weight in this claim drawn to structure. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

In regard to claim 42, wherein said impedance element comprises a first impedance element on said first side of said ceramic layer, further comprising a second impedance element on said second side of said ceramic layer. See Mashino's fig. 1.

5. Claims 24-26 and 40, 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino (US 6,545,353, newly cited) and Glenn and in view of Okabe et al. (US 2002/0118523, previously cited, hereinafter, Okabe.)

In regard to claim 24, Mashino and Glenn's combination discloses all of the claimed limitations as mentioned above, except an impedance element comprises a patterned inductor.

Okabe, in fig. 1, discloses an analogous device with stack substrate, multiple dielectric layers, 21, 22 and 23, and further teaches a patterned inductor 51 in order to obtain the control current and voltage supply to the chip.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the inductor in the substrate as taught by Okabe in order to control current and voltage supply to the chip.

In regard to claims 25-26, the processing limitations recited (diffusion, laser-trimmed, etc.), these would not carry patentable weight in this claim drawn to structure. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

In regard to claims 40 and 44, Okabe, in fig. 3, discloses an analogous device with stack substrate and further teaches a capacitor structure 52 on the polyimide film 21 in order to obtain the stabilization of the circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the capacitor in the substrate as taught by Okabe in order to stabilize the circuit since the structure prevents deterioration occurs therein.

In regard to claim 26, one of the patterns 106 may function as a ground pattern; see Mashino's fig. 1.

Response to Arguments

6. Applicant's arguments with respect to claims 18-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Nathan Ha
July 7, 2004

LONG PHAM
PRIMARY EXAMINER

LONG PHAM
PRIMARY EXAMINER